L Number	Hits	Search Text	DB	Time stamp
1	37	(semiconductor adj2 memory adj2 device) and (reference adj3 signal adj3 generator)	USPAT; EPO; JPO; DERWENT	2004/03/05 16:24
2	3	(semiconductor adj2 memory adj2 device) and (reference adj3 signal adj3 generator) and ((potential adj2 regulator) or (set$4 near3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:26
3	4	(semiconductor adj2 memory adj2 device) and (reference adj3 signal adj3 generator) and ((potential near4 regulat$4) or (set$4 near3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:29
4	4	(semiconductor adj2 memory adj2 device) and (reference adj3 signal adj3 generator) and ((potential near4 regulat$4) or (set$4 near3 potential) or (adjust$5 near3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:30
5	2143	(semiconductor adj2 memory adj2 device) and ((potential near4 regulat$4) or (set$4 near3 potential) or (adjust$5 near3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:30
6	439	(semiconductor adj2 memory adj2 device) same ((potential near4 regulat$4) or (set$4 near3 potential) or (adjust$5 near3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:30
7	794	(semiconductor adj2 memory adj2 device) same ((potential adj3 regulat$4) or (set$4 adj3 potential) or (potential adj3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:32
8	637	(semiconductor adj2 memory adj2 device) same ((potential adj3 regulat$4) or (potential adj2 set$4 adj2 up) or (potential adj3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:32
9	200	(semiconductor adj2 memory adj2 device) near10 ((potential adj3 regulat$4) or (potential adj2 set$4 adj2 up) or (potential adj3 potential))	USPAT; EPO; JPO; DERWENT	2004/03/05 16:33
10	1140	(semiconductor adj2 memory adj2 device) and ((potential adj3 regulat$4) or (potential adj2 set$4 adj2 up) or (potential adj3 potential)) and (signal adj2 generat$3)	USPAT; EPO; JPO; DERWENT	2004/03/05 16:34
11	20	(semiconductor adj2 memory adj2 device) and ((potential adj3 regulat$4) or (potential adj2 set$4 adj2 up) or (potential adj3 potential)) and (reference adj2 signal adj2 generat$3)	USPAT; EPO; JPO; DERWENT	2004/03/05 16:34
12	19	(semiconductor adj2 memory adj2 device) and ((potential adj3 regulat$4) or (potential adj2 set$4 adj2 up) or (potential adj3 potential)) and (reference adj2 signal adj2 generat$3) and amplif$5	USPAT; EPO; JPO; DERWENT	2004/03/05 16:49
13	1	reference adj2 potential adj2 set adj2 up adj2 circuit	USPAT; EPO; JPO; DERWENT	2004/03/05 16:53
14	3	potential adj2 set adj2 up adj2 circuit	USPAT; EPO; JPO; DERWENT	2004/03/05 16:53
15	27	potential adj2 regulating adj2 circuit	USPAT; EPO; JPO; DERWENT	2004/03/05 16:54
16	450	potential adj2 regulator	USPAT; EPO; JPO; DERWENT	2004/03/05 16:54
17	7	(potential adj2 regulator) same memory	USPAT; EPO; JPO; DERWENT	2004/03/05 16:57

18	6312	potential near3 arrang$5	USPAT; EPO; JPO; DERWENT	2004/03/05 16:58
19	2714	potential adj3 arrang$5	USPAT; EPO; JPO; DERWENT	2004/03/05 16:58
20	3234	(potential adj3 arrang$5) or (potential adj2 set adj2 up)	USPAT; EPO; JPO; DERWENT	2004/03/05 16:58
21	49	((potential adj3 arrang$5) or (potential adj2 set adj2 up)) same (semiconductor adj2 memory)	USPAT; EPO; JPO; DERWENT	2004/03/05 17:15
22	4346	ferroelectric adj2 memory	USPAT; EPO; JPO; DERWENT	2004/03/05 17:16
23	233	conventional adj3 (ferroelectric adj2 memory)	USPAT; EPO; JPO; DERWENT	2004/03/05 17:16
24	0	(conventional adj3 (ferroelectric adj2 memory)) and (potential adj2 set adj2 up adj2 circuit)	USPAT; EPO; JPO; DERWENT	2004/03/05 17:18
25	27	(conventional adj3 (ferroelectric adj2 memory)) and (potential adj4 circuit)	USPAT; EPO; JPO; DERWENT	2004/03/05 17:33
26	103	(ferroelectric adj2 memory) and (potential adj4 circuit)	USPAT; EPO; JPO; DERWENT	2004/03/05 17:33
27	103	(ferroelectric adj2 memory) and (potential adj4 circuit)	USPAT; EPO; JPO; DERWENT	2004/03/05 17:33